

Notice of References Cited

Application/Control No.

10/072,145

Applicant(s)/Patent Under
Reexamination
AVERETT ET AL.

Examiner

Thomas J. Magee

Art Unit

2811

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,640,041	06-1997	Water Lur et al.	257/510
	B	US-6,495,853 B1	12-2002	Allison Holbrook et al.	257/30
	C	US-2003/0030107	02-2003	Viktor Zekeriya	257/359
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)				
	U	S. Wolf, "Silicon Processing for the VLSI Era: Volume 2-Process Integration," Lattice Press, Sunset Beach, CA., (1990), pp. 196-197.				
	V					
	W					
	X					

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.